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SE-6227
B. E. - II (IC) (Sem. III) Examination
April / May – 2011
Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. - 2 (SEM. 3) (IC)**

Name of the Subject :

☛ **Digital Circuits**

☛ Subject Code No. : **6 2 2 7** ☛ Section No. (1, 2,.....) : **NIL**

Seat No. :

Student's Signature

1 Attempt all questions
2 Assume suitable data wherever required
3 Figure to the right indicate full marks.

1 (A) Answer the following questions **10**

(1) 1's complement of 10101010 is _____
(2) Draw the symbol and truth table of NOR gate
(3) Simplification of x+ xy is _____
(4) _____ is the gray code of 1011.
(5) _____is the binary equivalent of decimal number 111.
(6) What is the full form of ASCII ?
(7) What is the dual of A+AB ?
(8) Implement Y= AB +CD +E with the help of logic gates.
(9) 4 X 1 multiplexer has _____ selection lines.
(10) _____ and _____ are called universal gares.

1 (B) Explain Full adder circuit diagram and truth table. **6**

(C) Realize Ex- OR gate with NAND gates only. **4**

2 (A) Design binary to gray code converter circuit. **8**

(B) Simplify following boolean functions using K-map **7**
(1) F(a,b,c,d)= ∑m (1,5,7,9,11,13,15)
(2) F(w,x,y,z) = ∑m (1,3,4,5,7,9,11,13,15)

OR

2 (A) Simplify the following Boolean function using tabulation method **8**
F(A,B,C,D) =∑m (0,1,3,7,8,9,11,15)

(B) Design a combinational logic circuit whose out put is hogh only when majoriy of inputs (A,B,C,D) are low. **7**

3 Attempt any three. **15**

(1) Explain 3 to 8 line decoder with truth table and circuit diagram
(2) Implement following boolean function using 8 : 1 multiplexer
F(A,B,C,D) =∑m (2,4,5,7,10,14)
(3) Design 2 bit multiplier circuit.
(4) Explain BCD adder circuit.
(5) Design 3 bit parity generator and checker circuit.

Q4.

A) Attempt All.

1. Explain difference between 'Combination Circuit' and 'Sequential Circuit'. **[3]**

2. What do you mean by Race around condition? **[2]**

3. For J-K Flip- flop output is toggle when J = ____, K = _____. **[2]**

4. Differentiate Synchronous and asynchronous circuits. **[3]**

B) Explain 4-bit Ring Counter with necessary Wave forms. **[10]**

Q5. Attempt Any two. **[16]**

A) Explain Universal Shift register in detail.

B) Draw SR Latch circuit with Truth table ,Excitation table and Char. Equation.

C) Convert SR flipflop to JK Flipflop.

Q6. Attempt Any Two. **[14]**

A) Explain JK flipflop with Asynchronous inputs.

B) Explain ROM in Detail.

C) Design BCD Counter with JK flip flop.Draw necessary waveform.